Description

WF105RB is one low power direct-conversion OOK/ASK receiver. The circuit is mainly intended for the ISM (Industrial, Scientific and Medical) band 315/433MHz, it is designed for low cost data transmission system for data rate less than 40Kb/s in Manchester.

WF105RB integrates most circuit components on-chip and only requires a few external components to work normally. The WF105RB consists of a low-noise amplifier (LNA), a down-conversion mixer, an on-chip phase-locked loop (PLL) with integrated voltage-controlled oscillator (VCO) and loop filter, an ASK demodulator, a data filter, a data slicing comparator and an on-chip regulator.

The WF105RB is designed for low power and low voltage wireless applications. It is available in TSSOP-16 package and working over the extended temperature range (-40 to +85°C).

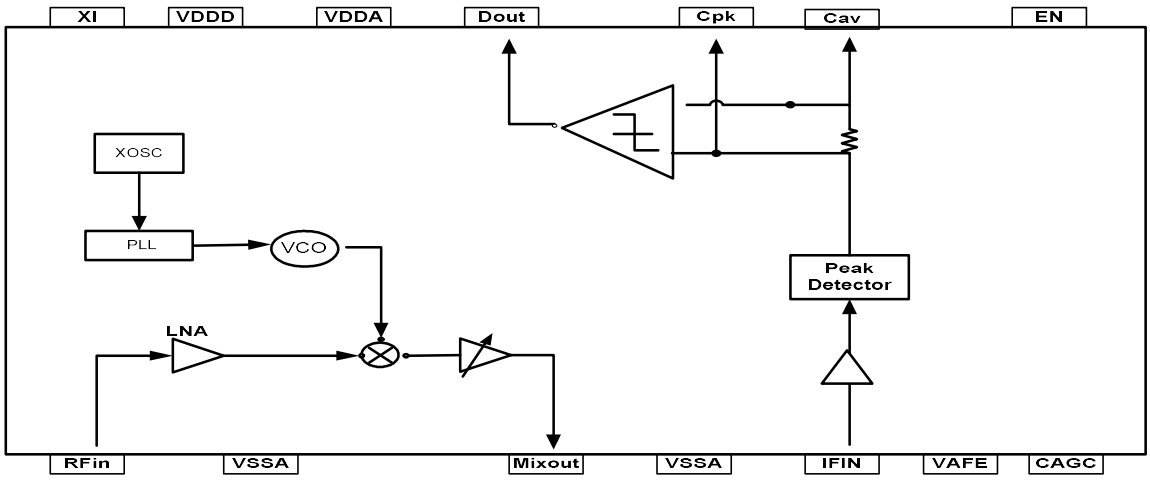
Features

- Low power consumption: 3.5mA for 315/433 MHz.
- Low supply voltage: 2.2V-5.5V for 315/433MHz.
- Excellent Sensitivity of the order of -110dBm (peak ASK signal level)
- 200 MHz to 500 MHz frequency range
- Data rate up to 40Kb/s

Applications

- Remote Keyless Entry (RKE)
- Remote Control, Garage door and gate openers
- AMR-Automatic Meter Reading
- Wireless alarm and security system.
- 315/433MHz ISM band system

Block Diagram



Pin Assignment

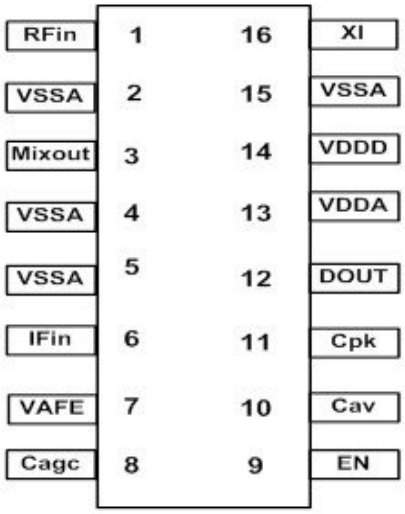


Table 1. Pin Description

Pin	Symbol	I/O	Description
1	RFin	I	RF input signal from antenna
2	VSSA	I/O	Ground
3	Mixout	O	IF output from Mixer, 300Ω output resistance, 10MHz typical
4	VSSA	I/O	Ground
5	VSSA	I/O	Ground
6	IFin	I	IF input, from external filter filtering IF output from Mixout
7	VAFE	I/O	Power supply for AFE part circuit
8	Cagc	I/O	External Cap for AGC, typ. value 1uF
9	**EN**	**I/O**	EN="1", enable chip, EN="0", Global power down chip. **default state "0"**
10	Cav	I/O	Connect to data slicing average cap. Typical 1uF.
11	**Cpk**	**I /O**	**IF peak signal average cap. Typ. 2nF**
12	Dout	O	Demodulated output data
13	VDDA	I/O	LDO output, used for AFE Power supply, pin 7

14	VDDD	I/O	Power supply for digital output part circuit (2.2V-5.5V).
15	VSSA	I/O	Ground
16	XI	O	Input terminal of local oscillation signal. It is connected to the crystal or driven by an external clock.

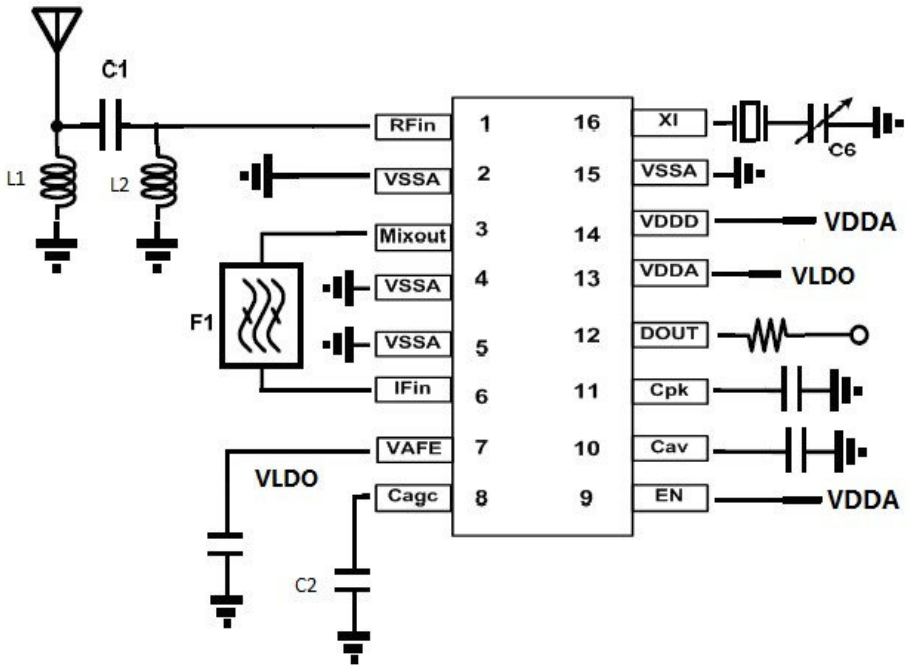
Table 2. Absolute Maximum Rating

Item	Rating
Supply Voltage, VDD	+ 6.0V
Inputs and Clock Outputs	- 0.5V to + 6.0V
Storage Temperature	- 65 °C to + 150 °C
Soldering Temperature	+ 260 °C

Table 3. Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Regulated Voltage	V_{DDA}			2.6		V
Supply Voltage	V_{DDD}	200MHz-500MHz	2.2	3.0	5.5	V
Supply Current	I_{DD}	Fin=315MHz , 3V		3.5		mA
		Fin=434MHz , 3V		3.6		mA
FIN operating Frequency	Fin		200		500	MHz
FIN Sensitivity	V_{FIN}	Fin=315MHz		-110		dBm
		Fin=433MHz		-110		dBm
OSCI operating Frequency	F_{OSC}		9		25	MHz
OSCI Input Voltage	V_{OSCI}		-10	0	5	dBm
Operating Temperature	T_a		-40		85	℃
Leakage Current	I_{SB}	Power down mode			10	uA

Typical Application Circuit —Heterodyne Receiver



	315MHz	433MHz	Note
L1	56nH	56nH	
L2	68nH	39nH	
C1	1.5pF	1.2pF	

Functional Description

Crystal Oscillator (Pin 16)

The crystal oscillator circuit consists of a colpit oscillator. Pin 16 can drive one off-chip 9MHz-25MHz

The crystal driver stage can also take input clock as input clock buffer. The crystal oscillator frequency is determined as follows

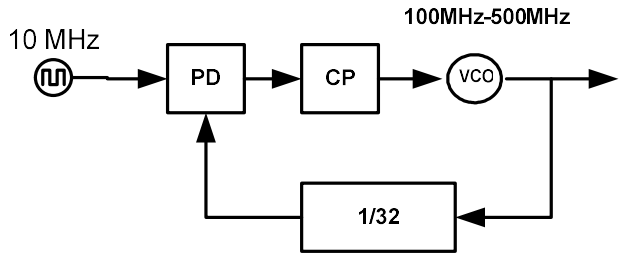
fosc= fvco / N = (ftx +/- 10.7) / N

Where Fvco is VCO oscillation frequency. Ftx is the transmitted/received signal frequency. 10.7MHz is super-heterodyne receiver IF frequency. N is the divider ration of PLL block.

PLL Block

The below figure shows the PLL block diagram. The PLL consists of phase-frequency detector (PFD), charge pump, loop filter, voltage-controlled oscillator (VCO), divider (1/32), and output stage frequency doubler. The PFD compares two signals and produces an error signal which is proportional to the two signal phase difference. The error signal is used to control the VCO to run fast or slow. The frequency doubler is used to double the output signal frequency.

The VCO oscillation frequency range is tunable between100MHz-500MHz,



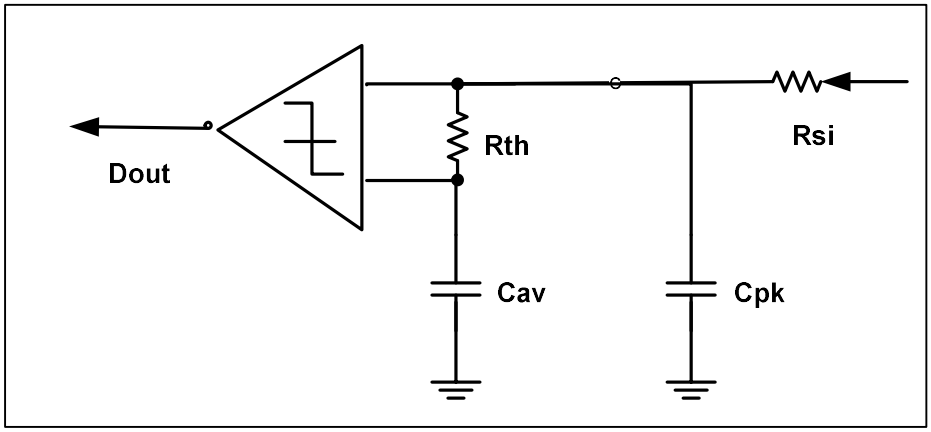
Peak-Detector & ASK Demodulator

The peak-detector detects the HIGH and LOW modulated ASK signal level. The ASK demodulation is done by data slicer.

The data slicer takes the input analog signal from peak detector and determines the input signal is HIGH or LOW. The reference level for data slicer slicing is the long-term average of peak-detected signal, using the external threshold capacitor **C_{AV}** (pin 10) and the on-chip resistor R_{TH}, which is about **30KΩ**. The

Slicing level time constant values (**$T = C_{AV} * R_{TH}$**) can be set around 10X bit period time.

To reduce the variation of peak-detected signal, an external capacitor **C_{pk}** (pin 11) is used to reduce the ripple. The time constant values (**$T = C_{pk} * R_{SI}$**) can be set around 1X bit period time. The internal resistance **R_{SI}** is around **60K.**



For 1Kb/s data rate, the typical value **C_{AV} =1000nF, C_{pk} =1nF.**

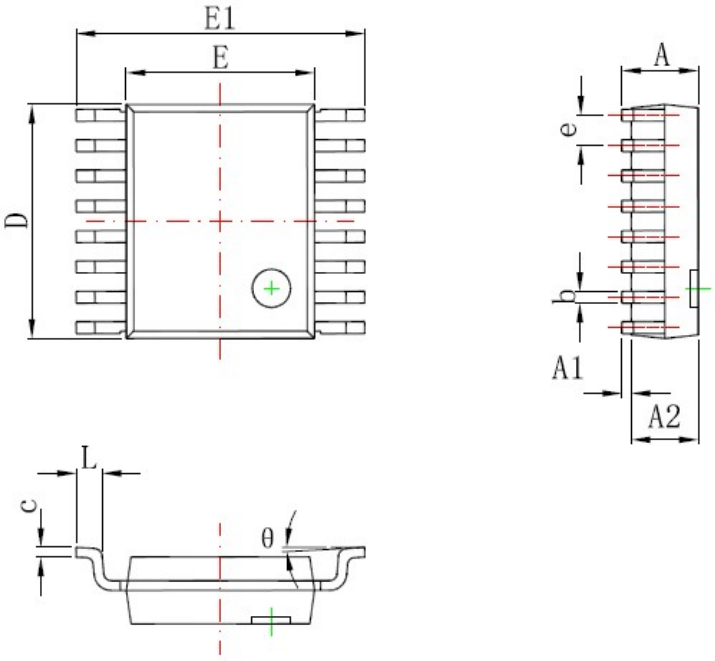
Below table is suggested capacitor value for different data rate.

Slicer cap	Bit Rate		Note
	10Kb/s	1KB/s	
Cav	1000n	1000n	
Cpk	0.1n	1n	

AGC Loop

The AGC loop compares HIGH signal level with average signal. When the signal difference is larger than 50mV, the AGC loop reduces the analog front end (AFE) stage gain. The external capacitor Cagc controls the AGC loop response time.

Package Information TSSOP-16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.200	0.300	0.008	0.012
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	0.635(BSC)		0.025(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°